# CLAIMS

1. An integrated circuit, comprising:

an input port by which data is received from a source external to the integrated circuit;

a configurable logic array having a programmable configuration defined by configuration data stored in electrically programmable configuration points within the configurable logic array;

memory adapted to store instructions for a mission function for the integrated circuit, to store instructions for a configuration load function used to receive configuration data via said input port, and to store instructions for a configuration function used to transfer the configuration data to the programmable configuration points within the configurable logic array;

a processor coupled to the memory which fetches and executes instructions from the memory.

2. The integrated circuit of claim 1, wherein said memory comprises a nonvolatile store.

3. The integrated circuit of claim 1, wherein said memory comprises a floating gate memory store.

4. The integrated circuit of claim 1, wherein said memory comprises a read-only memory store.

5. The integrated circuit of claim 1, wherein said memory comprises a first nonvolatile store for the configuration function, and a second store for the mission function.

6. The integrated circuit of claim 1, wherein said memory comprises a first programmable, nonvolatile store for the configuration load function, and a second store for the mission function.

7. The integrated circuit of claim 1, including a watchdog timer coupled to the processor, and wherein the configuration function includes using the watchdog timer to generate a reset in response to errors, and upon the reset, re-executing the configuration load function and the configuration function.

8. The integrated circuit of claim 1, including a watchdog timer coupled to the processor, and wherein the configuration load function includes using the watchdog timer to generate a reset in response to errors, and upon the reset, re-executing the configuration load function.

9. The integrated circuit of claim 1, wherein the configuration load function includes receiving encrypted configuration data via an input port on the integrated circuit, and decrypting the configuration data.

10. The integrated circuit of claim 1, wherein the configuration load function includes receiving compressed configuration data via an input port on the integrated circuit, and decompressing the configuration data.

11. The integrated circuit of claim 1, wherein the electrically programmable configuration points comprise floating gate memory cells.

12. The integrated circuit of claim 1, wherein the electrically programmable configuration points comprise nonvolatile, charge programmable memory cells.

13. The integrated circuit of claim 1, wherein the electrically programmable configuration points comprise nonvolatile, programmable memory cells.

14. The integrated circuit of claim 1, including:

an interface between the processor and the configurable logic array supporting said configuration load function.

15. The integrated circuit of claim 1, wherein said memory stores instructions for an in-circuit programming function to write or modify instructions for the configuration load function.

16. The integrated circuit of claim 1, wherein said memory includes a protected memory array storing instructions for a first configuration load function, and a second memory array storing instructions for a second configuration load function, the first memory array being protected from alteration by an in-circuit programming function and the second memory array being accessible to be written or modified by the in-circuit programming function.

17. The integrated circuit of claim 1, wherein said processor comprises a configurable logic array configured to execute said instructions.

18. A method for providing for error recovery during loading of configuration data to an integrated circuit including a processor, a configurable logic array having configuration points to store the configuration data, and memory storing instructions executable by the processor including instructions for a configuration load function to load configuration data from a source external to the integrated circuit, comprising:

monitoring the loading of configuration data using the configuration load function in order to detect a delay in transmission of configuration data from a remote host; and

restarting the configuration load function if the delay exceeds a timeout value.

19. The method of claim 18, wherein the step of monitoring is performed by using a watch dog timer on the integrated circuit and coupled to the processor.

20. A method for configuring an integrated circuit including a processor, a configurable logic array having a programmable configuration defined by configuration data stored in electrically programmable configuration points within the configurable logic array, and memory storing instructions executable by the processor, the method comprising:

storing instructions in a first memory array of said memory for a mission function for the integrated circuit;

storing instructions in a second memory array of said memory for configuration load function used to receive configuration data from a source external to the integrated circuit; and

storing instructions in a third memory array of said memory for a configuration function used to transfer the configuration data to the programmable configuration points within the configurable logic array.

21. The method of claim 20, wherein said memory comprises a nonvolatile store.

22. The method of claim 20, wherein said memory comprises a floating gate memory store.

23. The method of claim 20, wherein said memory comprises a read-only memory store.

24. The method of claim 20, wherein said second array of said memory comprises a first nonvolatile store for the configuration function, and first array of said memory comprises a different second store different than the first nonvolatile store for the mission function.

25. The method of claim 20, wherein said second array of said memory comprises a first programmable, nonvolatile store for the configuration function, and first array of said memory comprises a different second store different than the first nonvolatile store for the mission function.

26. The method of claim 20, wherein the configuration load function includes receiving encrypted configuration data via an input port on the integrated circuit, and decrypting the configuration data.

27. The method of claim 20, wherein the configuration load function includes receiving compressed configuration data via an input port on the integrated circuit, and decompressing the configuration data.

28. The method of claim 20, wherein the electrically programmable configuration points comprise floating gate memory cells.

29. The method of claim 20, wherein the electrically programmable configuration points comprise nonvolatile, charge programmable memory cells.

30. The method of claim 20, wherein the electrically programmable configuration points comprise nonvolatile, programmable memory cells.

31. The method of claim 20, including:

monitoring the loading of configuration data using the configuration load function in order to detect a delay in transmission of configuration data from a remote host; and

restarting the configuration load function if the delay exceeds a timeout value.

32. The method of claim 20, including:

monitoring the loading of configuration data using a watch dog timer on the integrated circuit and coupled to the processor during the configuration load function in order to detect a delay in transmission of configuration data from a remote host; and

restarting the configuration load function if the delay exceeds a timeout value.